ACQ400 FIR Filters Guide

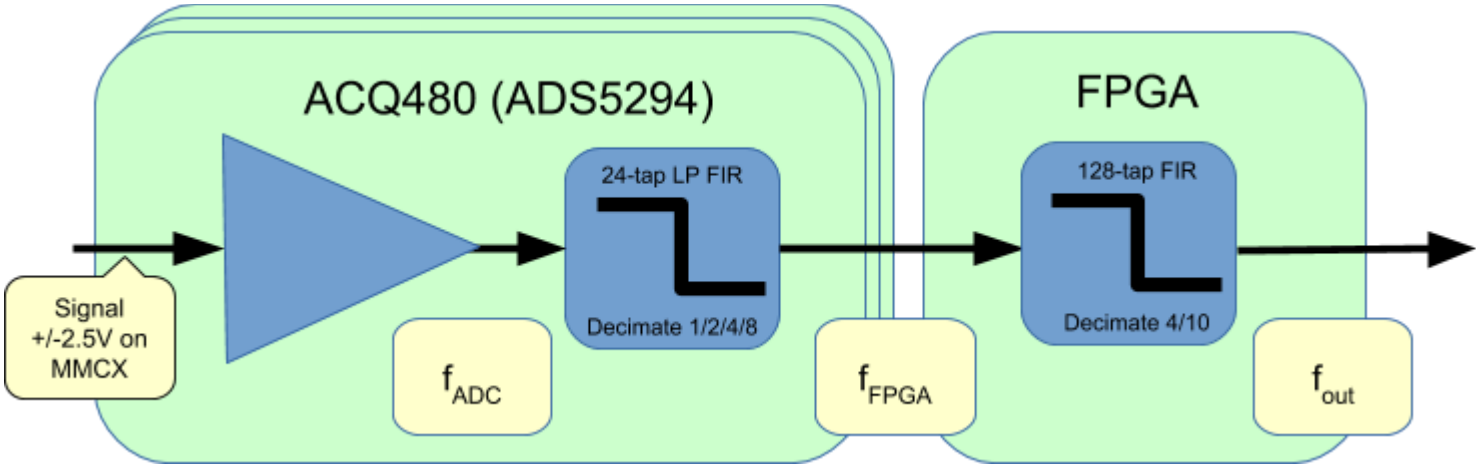
This document describes the FPGA FIR Filter implementation on D-TACQ ACQ400 Series products. An overview of the filters and the steps required for end users to control them is given.

D-TACQ Filter Architecture Block Diagram

The ACQ480 filtering is split into two stages. There is a small programmable FIR filter on the ADC device itself, and a larger, more capable FIR filter implemented in the FPGA fabric.

This provides two stages for potential decimation and data reduction, whilst the ADCs are still sampling at full rate.

The various sampling rates throughout the decimation change are named as indicated below. These names are useful when providing worked examples; included later in this document.



ACQ480 ADS5294 FIR Filters

The ADS5294 ADC has some DSP features on board. These include built in FIR decimating filters.

Filter Characteristics

- 24 taps
- Symmetric
- 12-bit Signed coefficients
- 9 (Input) Clock Latency (in addition to the standard 11 clock ADC pipeline)
- Decimation?
    - Decimate by 1, 2, 4 & 8

ACQ480 FPGA FIR Filters

The ACQ480 product utilises hardware FIR filters in the FPGA logic as a means to reduce the data rate, through oversampling, or to make SNR improvements through narrowing the signal bandwidth.

Filter Characteristics

- Maximum Sample Rate
    - ACQ1001 - 32 MHz
    - ACQ2106 - 40 MHz
- 128 taps
- Symmetric
- 20-bit Signed coefficients
- Latency
    - DEC4 = 34 (Input) clock cycles, DEC10 = 55 (Input) clock cycles
    - Post decimation this equates to DEC4 = 8.5, DEC10 = 5.5
- Decimation
    - There are two FPGA personalities
    - Decimate by 4 or Decimate by 10 (DEC4 or DEC10).
    - This is a boot time switch explained in Setup Example later in document.
- **Default (no coefficient reload) cutoff frequency is at Nyquist**

D-TACQ provide several coefficient files allowing the end user to tailor the response of the filters. Plots of the provided filter responses are included in the Appendix.

Setup Filter Coefficients

In order to begin using the filtering options presented above a support package must first be installed. A user can access the D-TACQ command line over ssh or through a serial comms connection.

A full scripted example of filter configuration is included in the Appendix.

Install Package

Move the new package to the /mnt/packages directory and reboot the D-TACQ box.

```
mv /mnt/packages.opt/90-custom_acq480fir* /mnt/packages
```

A new directory is created at `/usr/local` called **coeff_sets**.

This contains a set of useful coefficients for each FIR.

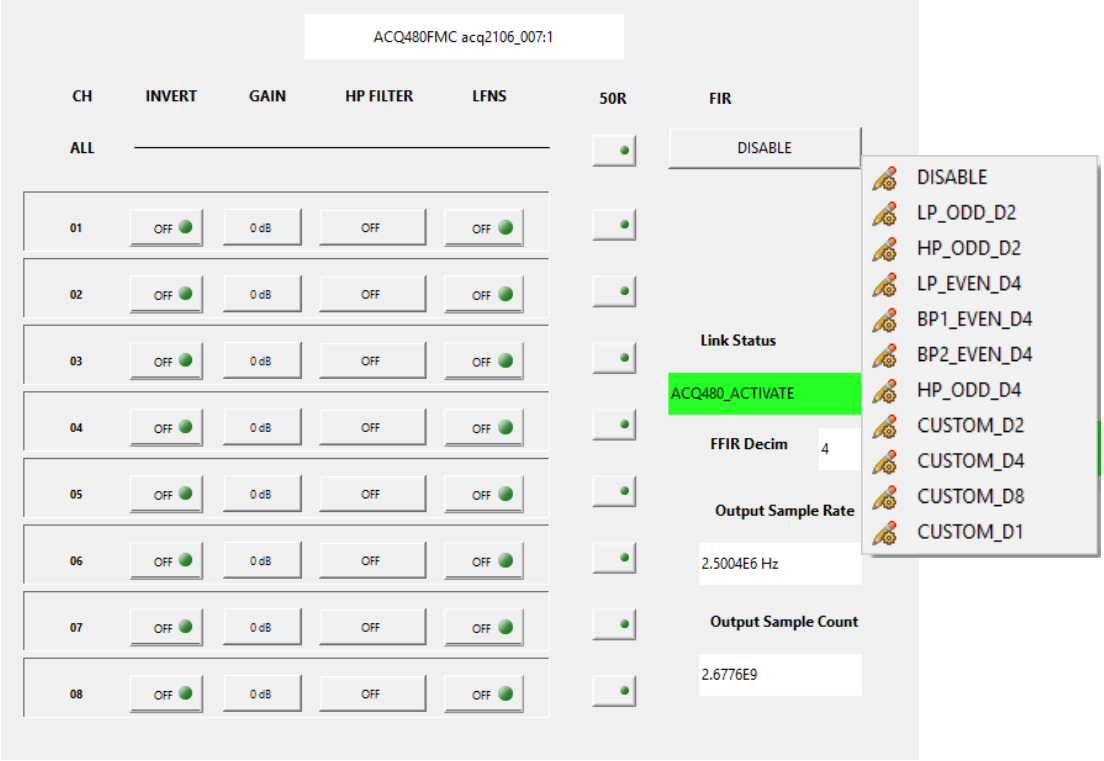
```
ADS5294:
total 192
-rwxr-xr-x    1 root     root            75 Aug  5 14:22 by16
-rwxr-xr-x    1 root     root            76 Aug  5 14:22 by32
-rwxr-xr-x    1 root     root            75 Aug  5 14:22 by4
-rwxr-xr-x    1 root     root            75 Aug  5 14:22 by8
-rwxr-xr-x    1 root     root            58 Aug  5 14:22 half_amp
-rwxr-xr-x    1 root     root            59 Aug  5 14:22 unity_gain

DEC10:
total 128
-rwxr-xr-x    1 root     root           387 Aug  5 14:22 nyquist
-rwxr-xr-x    1 root     root           165 Aug  5 14:22 half_gain
-rwxr-xr-x    1 root     root           377 Aug  5 14:22 half_nyq
-rwxr-xr-x    1 root     root           165 Aug  5 14:22 unity_gain

DEC4:
total 96
-rwxr-xr-x    1 root     root           353 Aug  5 14:22 nyquist
-rwxr-xr-x    1 root     root           133 Aug  5 14:22 half_gain
-rwxr-xr-x    1 root     root           350 Aug  5 14:22 half_nyq
-rwxr-xr-x    1 root     root           133 Aug  5 14:22 unity_gain
```

Select Custom ADS5294 Filter Decimation

From Control System Studio (CSS) open the ACQ480 opi for the relevant site.



The list of default filters are shown in the dropdown menu. The default filter responses for these filters are shown in the Appendix

The bottom 4 options in the dropdown menu, with prefix CUSTOM, allow the user to select a decimation factor (1,2,4,8) and apply the custom filter coefficients which will be loaded in the next step.
Note the “FFIR (FPGA FIR) Decim” field reports the internal decimation within the FPGA. **This is controlled by loading a specific named FPGA bitstream.**

Or set programmatically

```
set.site 1 ACQ480:FIR:01 FILTYPE
```

Where FILTYPE : one of {
DISABLE,
LP_ODD_D2, HP_ODD_D2,
LP_EVEN_D4, BP1_EVEN_D4, BP2_EVEN_D4, HP_ODD_D4,
CUSTOM_D2, CUSTOM_D4, CUSTOM_D8, CUSTOM_D1 }

Loading Coefficients

FPGA Filter Load

To load a coefficient set into the FPGA FIR execute the following line :

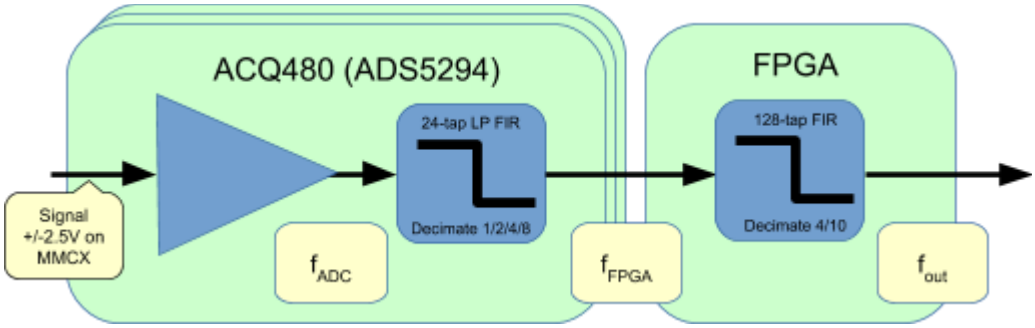
```
/usr/local/CARE/load.ffir /usr/local/coeff_sets/DECX/half_nyq
using file /usr/local/coeff_sets/DEC4/half_nyq
```

ADS5294 Filter Load

To load a coefficient set into the ADS5294 FIR, load any of the supplied coefficient sets from /usr/local/coeff_sets/ADS5294 by name (or specify another file name to load custom settings).

```
/usr/local/CARE/load.acq480.fir by8
```

In the above example, the by8 coefficient set describes a filter whose cut-off begins at 1/8th of the ADC's input sampling frequency (f_{ADC}). The various filter coefficients can be combined with the decimation rate to produce (referenced to the final sampling frequency f_{out}) Nyquist or half Nyquist cutoff points.



f_{ADC}	ADS5294 Decimation (f_{FPGA})	ADS5294 Coeff Set	ADS5294 Cutoff frequency	FPGA Decimation (f_{out})	FPGA Coeff Set	FPGA Cutoff frequency
80 MHz	4 (20 MHz)	by32	2.5 MHz	0	N/A	N/A
	2 (40 MHz)	by16	5 MHz	4 (10 MHz)	nyquist	5 MHz
40 MHz	0	N/A	N/A	10 (4 MHz)	half_nyqt	1 MHz
	2 (20 MHz)	by16	2.5 MHz	4 (5 MHz)	nyquist	2.5 MHz
20 MHz	2 (10 MHz)	by32	625 kHz	10 (1 MHz)	half_nyq	250 kHz

Filter response plots are provided in the Appendix.

Custom User Coefficients

It’s possible for users to roll their own filter coefficients. Contact D-TACQ for details.

Appendix

ADS5294 Default Coefficient Filter Response

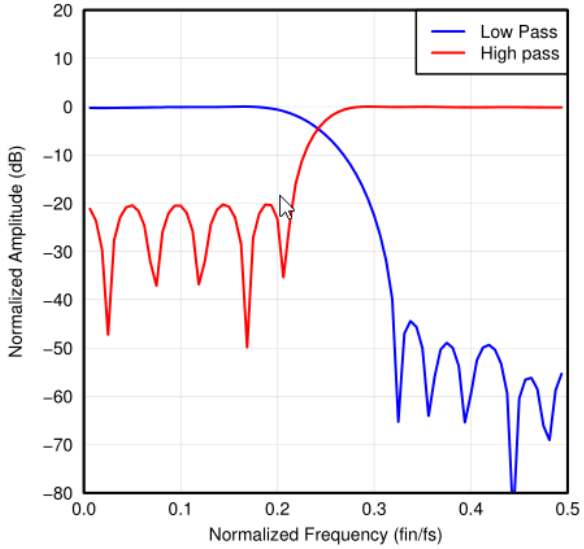


Figure 48. Decimation Filter Responses (Decimate by 2)

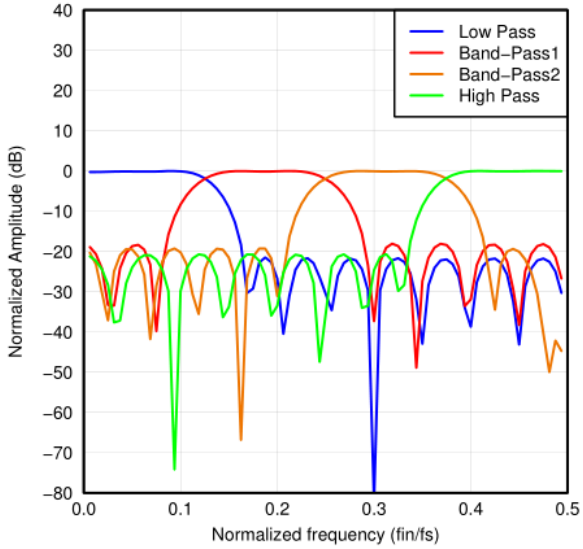
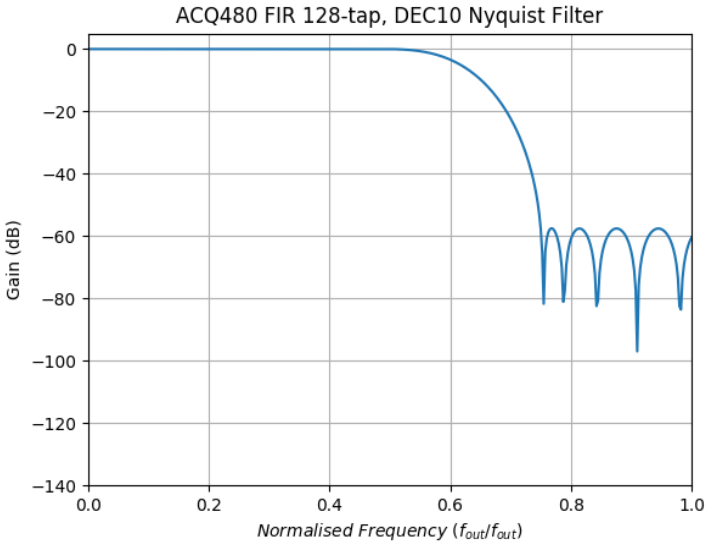


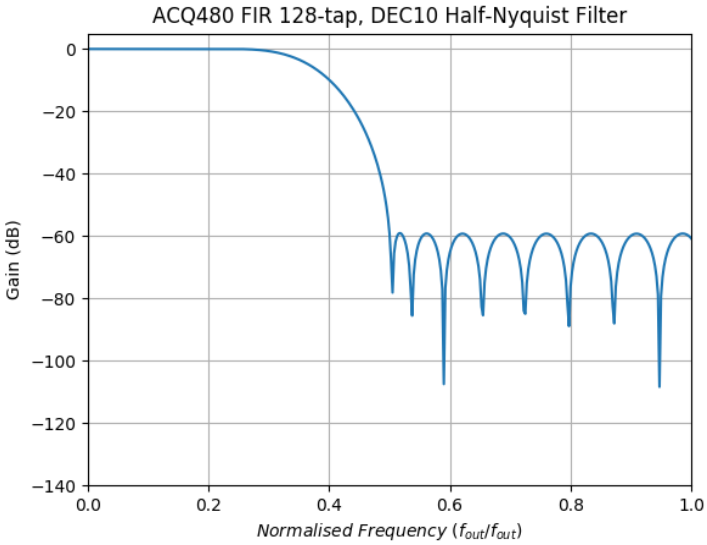
Figure 49. Decimation Filter Responses (Decimate by 4)

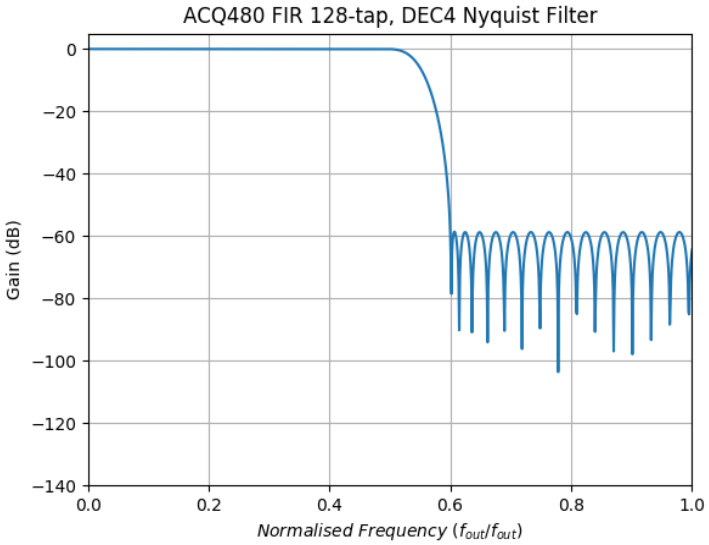
FPGA FIR Coefficient Filter Responses

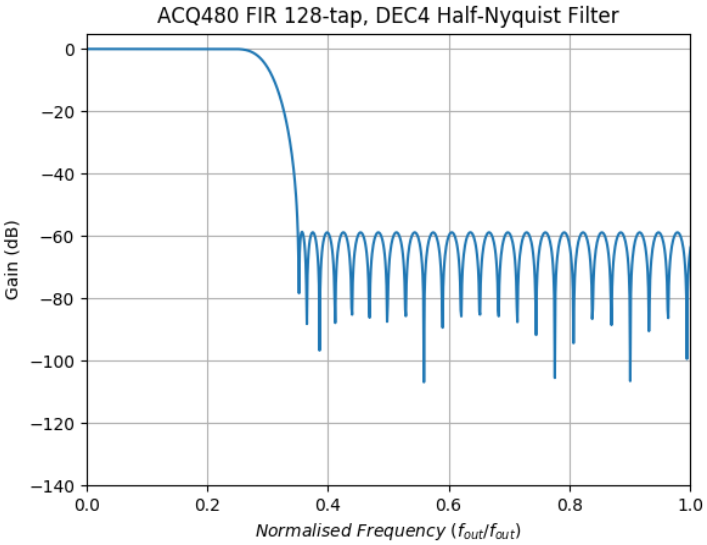
- N.B. The 128 tap FPGA filter responses are plotted against normalised output frequency (f_{out}). Half of the Normalised Frequency is equal to the Nyquist rate.

DEC10 Nyquist - 128tap_by20, coeff_sets/DEC10/nyquist
DEC10 Half-Nyquist - 128tap_by40, coeff_sets/DEC10/half_nyq
DEC10 Nyquist - 128tap_by8, coeff_sets/DEC4/nyquist
DEC10 Nyquist - 128tap_by16, coeff_sets/DEC4/half_nyq



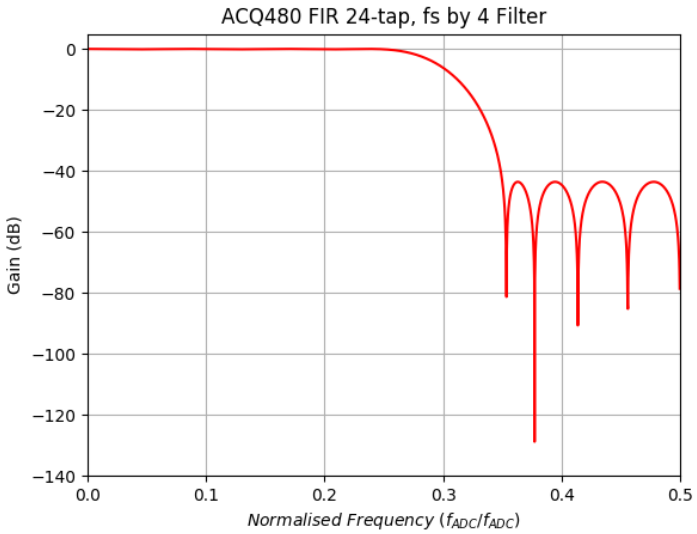


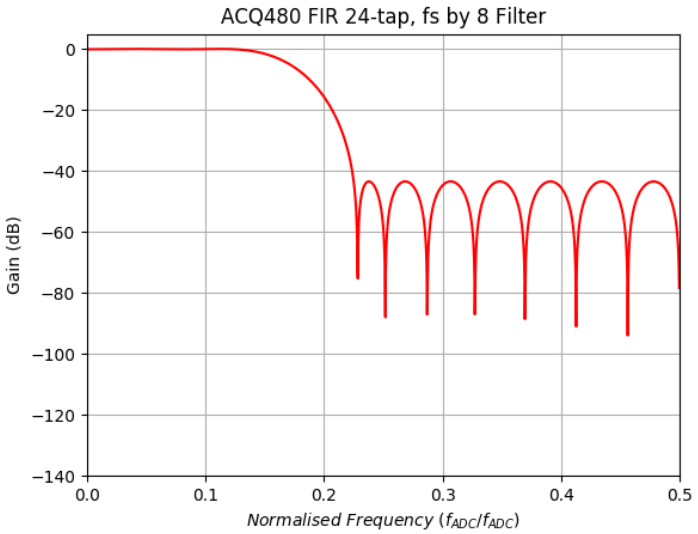


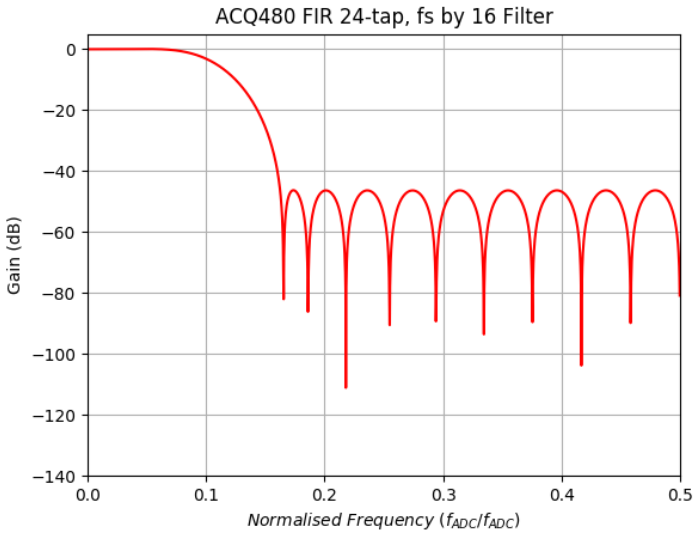


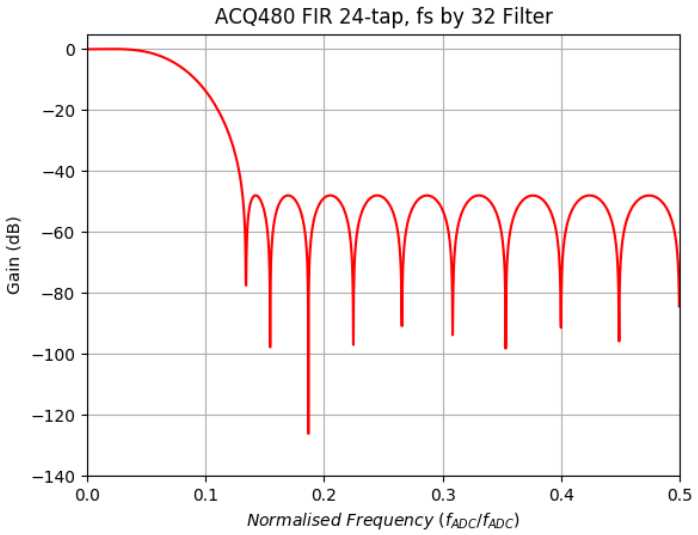
ADS5294 Custom Coefficient Filter Response

- N.B. The 24 tap ADC filter responses are plotted against normalised input frequency (f_{ADC}) i.e. ADC sample clock rate. The decimation on the ADC filters are configurable so it is clearer to specify the response against this quantity.

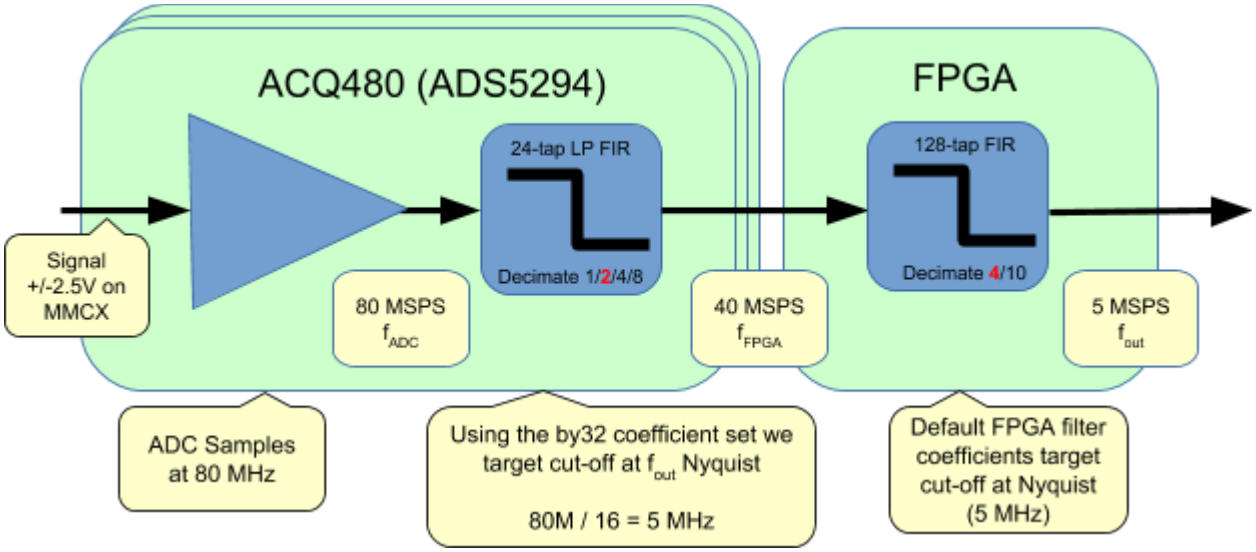








Example Configuration Script



- Sampling Rate *or* f_s *or* f_{ADC} = 80 MHz
- ADS5294 Decimation = 2
- Decimated ADS5294 Rate *or* f_{FPGA} = 40 MHz
- FPGA Decimation = 4
- Decimated FPGA Rate *or* f_{out} = 10 MHz

To replicate the above example we need to :

1. Load the correct DECX FPGA
    a. In this case we would like a decimation factor of 4 so must select DEC4 FPGA
2. Apply a suitable FPGA FIR coefficient set
3. Select the ADS5294 Decimation
4. Apply a suitable ADS5294 coefficient set

1. FPGA Selection and Preferential Load

FPGA images located at /mnt on the D-TACQ ACQ400 device will skip the usual FPGA arbitration process and (assuming it is safe) will load preferentially.

It is necessary to promote either the DEC4 or DEC10 FPGA depending on what the end user's application.

To promote an FPGA, ssh into the ACQ400 device and copy it from /mnt/fpga.d to /mnt and reboot the unit under test.

```
cp /mnt/fpga.d/ACQ*08*9011*DEC4.bit.gz /mnt; sync;sync;reboot
```

When the box has rebooted the remaining steps can be completed.

2. Applying a suitable FPGA FIR Coefficient Set

```
/usr/local/CARE/load.ffir /usr/local/coeff_sets/DEC4/half_nyq
```

3. Selecting the ADS5294 Decimation

```
set.site 1 ACQ480:FIR:01 CUSTOM_D2
```

4. Applying a suitable ADS5294 Coefficient Set

```
/usr/local/CARE/load.acq480.fir by16
```