ACQ430FMC Product Specification

High Performance Simultaneous Data Acquisition

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Subject to change

Contents

Revision History

Revision	Date	Author(s)	Description
3	January 2015	JMcL	Updated Performance Figures
4	January 2024	JMcL	Updated to current template, updated carrier support, added LFP versions, added FMC Design Details

Glossary

- FMC : VITA57.1 FPGA Mezzanine Card
- ELF : Electrically Extended FMC, implies ULPC or DULPC (only compatible with D-TACQ carriers)
- LPC : FMC Low Pin Count standard as per VITA57.1
- ULPC : Subset by D-TACQ, Ultra Low Pin Count
- DULPC : Subset by D-TACQ, Differential Ultra Low Pin Count (ULPC with extra differential signalling)
- Xilinx ZYNQ System on Chip (SoC)
- FPGA : Field Programmable Gate Array

1 Product Description

- ACQ430FMC is an 8 channel, 24 bit simultaneous analog input module
- Standard configuration : 8 channels, 125 kSPS/channel
- 2-wire Differential inputs, high quality differential amplifier front end

1.1 Product Variants

- ACQ430FMC 8 channels, FMC compliant, 36 way MDR (Mini-Centronics) Connector
- ACQ430ELF 8 channels, D-TACQ ELF compliant, 36 way MDR (Mini-Centronics) Connector
- ACQ430FMC-4-LFP 4 channels,FMC compliant , 4 single Pin LEMO connectors
- ACQ430FMC-8-LFP 8 channels, D-TACQ ELF compliant, 4 single Pin LEMO connectors on Front Panel, 4 single Pin LEMO connectors on Top Deck. Can be used with the PandABox [1]
- Please contact info@d-tacq.com for other Front Panel connection options

1.2 Applications

- Instrumentation applications, control and monitoring.
- Acoustic and seismic applications.

1.3 Carrier Compatibility

The FMC module standard adds user IO to carrier modules fitted with FPGA resource. D-TACQ recommends modules based on the Xilinx ZYNQ system on chip, combining FPGA resource with ARM CPU and Gigabit Ethernet.

The ELF module standard is a D-TACQ standard and is compatible with only D-TACQ Carriers.

Compatible carriers include:

- D-TACQ ACQ1001 : D-TACQ single slot FMC carrier, Z7020
- D-TACQ ACQ1002 : D-TACQ dual slot FMC carrier, Z7020
- D-TACQ ACQ2106 : D-TACQ 6 slot FMC carrier, Z7030
- D-TACQ ACQ2206 : D-TACQ 6 slot FMC carrier, Z7030
- D-TACQ ACQ1102 : D-TACQ 2 slot FMC carrier, Z7030
- DAMC-FMC1Z7IO + D-TACQ ACQ400-MTCA-RTM-2

D-TACQ supplies a complete working Intelligent Digitizer appliance including programmable logic and micro-processor system running Linux.

[1] PandABox (Position and Acquisition Box) is a collaboration between SOLEIL and DIAMOND see OHWR PandABox

2 Physical

2.1 Board Outline

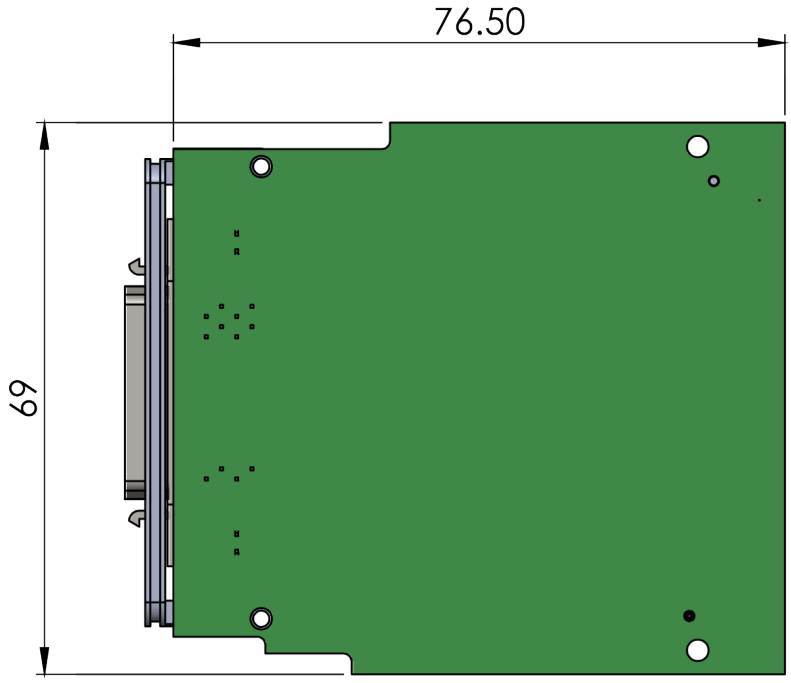

Figure 1: Board Outline

2.2 Appearance

The picture below shows the ACQ430FMC board with the 36 way MDR (Mini-Centronics) Connector

Figure 2: ACQ430FMC Board Appearance

The picture below shows the ACQ430FMC-8-LFP board with dual stacked 4 pin LEMO top Deck

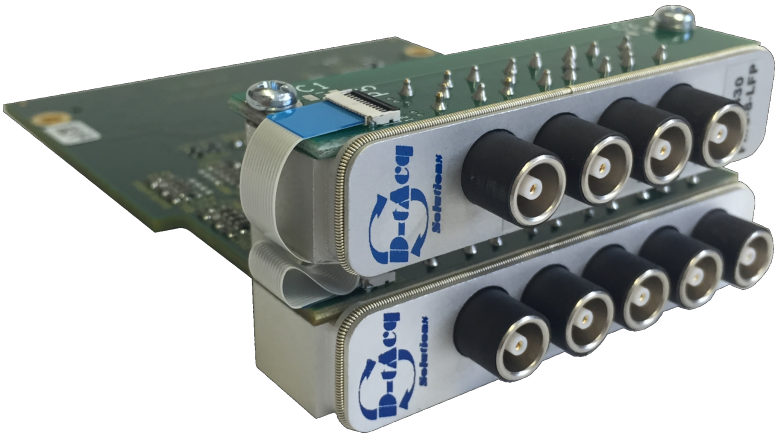

Figure 3: ACQ430FMC-8-LFP Board Appearance

2.3 Front Panel Connector & Pinout

2.3.1 36 Pin MDR (Mini-Centronics)

- 36 Pin MDR (Mini-Centronics) 3M 10236-55G3PL
- Mating Part 3M 10136-6000EL
- Compatible cables include: Videk 1082-2

Pin	Function	Pin	Function
1	0V	19	0V
2	CH_08+	20	CH_08-
3	0V	21	0V
4	CH_07+	22	CH_07+
5	+12V	23	+5V
6	TRIG	24	CLK
7	0V	25	0V
8	CH_06+	26	CH_06-
9	0V	27	0V
10	CH_05+	28	CH_05-
11	0V	29	0V
12	CH_04+	30	CH_04-
13	0V	31	0V
14	CH_03+	32	CH_03-
15	0V	33	0V
16	CH_02+	34	CH_02-
17	0V	35	0V
18	CH_01+	36	CH_01-

Table 1: Front Panel 36 Pin MDR Pinout

2.3.2 Single Pin LEMO

- Single-pin LEMO 00 Series Mini Coax connector (part EPL.00.250.NTN)
- Mating Part FFA.00.250.NTAC29

Pin	Function	Pin	Function
Centre	CHANNEL +ve	Shell	CHANNEL -ve

Table 2: Front Panel LEMO Connectors Pinout

3 Electrical Specification

The table below is for the 32 I/O signals

#	Parameter	Value
1	Number of Channels	8
2	Sample Rate High Speed Mode High Resolution Mode	Per channel simultaneous 125 kHz 52 kHz
3	Resolution	24 bits
4	Coupling	DC, Differential Input
5	Input Impedance	1 MΩ
6	Input Voltage Range	±10 V [1]
7	Input Voltage Withstand	±30 V
8	Offset Error	0.01% FS with numerical calibration
9	Gain Error	0.01% FS with numerical calibration
10	INL	±0.002% FS
11	Analog Input BW	80 kHz
12	CMRR	> 60 dB FS @ 1 kHz
13	Crosstalk	< 90 dB @ 1 kHz FS Input
14	THD	-106 dB [2]
15	SFDR	107 dBc [2]
16	Sample Rate High Speed Mode High Resolution Mode	 104 dB [2] 108 dB [2]
17	Digital Filter:Pass Band Digital Filter:3dB Digital Filter:Stop Band Digital Filter:Attenuate	0.453 Fsample 0.490 Fsample 0.547 Fsample 95 dB

[1] Custom Input Voltages available please contact info@d-tacq.com for details
[2] Typical values measured at full scale with a 9.76kHz input

Table 3: ACQ430FMC Electrical Performance

The optional dedicated input clock buffer has the same input voltage characteristics as the 32 I/Os

4 Mechanical,Power & Environmental Specification

#	Parameter	Value
1	Form Factor	Standard FMC
2	Power Source	DC 12V, 200 mA DC 3.3V, 100 mA
3	Environmental	0 °C - 50 °C Operational −10 °C - 85 °C Non-Operational
4	Mezzanine Socket	Standard FMC, Low Pin Count LPC

Table 4: Mechanical & Environmental Specification

A FMC Information

The ACQ430FMC uses the Texas Instruments ADS1278 24 bit ADC, please review the data-sheet for using this device.

A.1 I^{2}C Devices

The board is fitted with 2 I^{2}C devices as follows

Address	Device	Description
0x28	AD7417	Temperature Sensor and Analog Input
0x50	M24C64	Serial IPMI FRU PROM

Table 5: I^{2}C devices

A.1.1 AD7417 Temperature Sensor

See the data sheet at AD7417

A.1.2 Serial IPMI FRU PROM

This is a standard FMC FRU devices the contents of the PROM are as per the FMC standard and the *IPMI Platform Management FRU Information Storage Definition v1.0*

Below is an example of a ACQ430FMC module with the serial number 10.

```
../fru-dump  E48220010.fru
header 0x1b88010 bia 0x1b88018
E48220010.fru: manufacturer: D-TACQ Solutions
header 0x1b88010 bia 0x1b88018
E48220010.fru: product-name: ACQ430FMC
header 0x1b88010 bia 0x1b88018
E48220010.fru: serial-number: E48220010
header 0x1b88010 bia 0x1b88018
E48220010.fru: part-number: ACQ430FMC N=32 M=6B
```

A.2 FMC Connector Pinout

Pin	Signal Name	Description
p_FMC_CLK0_M2C_p	EXT_CLK	External Clock
p_FMC_CLK0_M2C_n	Not Used	Not Used
p_FMC_LA00_CC_p	ADC_MODE_0	ADC_MODE_0
p_FMC_LA00_CC_n	Not Used	Not Used
p_FMC_LA01_CC_p	Not Used	Not Used
p_FMC_LA01_CC_n	Not Used	Not Used
p_FMC_LA02_p	FP_SCL	Optional I2C Bus SCL (MDR 36 Only)
p_FMC_LA02_n	Not Used	Not Used
p_FMC_LA03_p	FP_SDA	Optional I2C Bus SDA (MDR 36 Only)
p_FMC_LA03_n	Not Used	Not Used
p_FMC_LA04_p	ADC_FSYNC	ADC_FSYNC
p_FMC_LA04_n	Not Used	Not Used
p_FMC_LA05_p	RIBBON_PRSNT_n	TOP Deck Ribbon Present (LPC Only)
p_FMC_LA05_n	Not Used	Not Used
p_FMC_LA06_p	Not Used	Not Used
p_FMC_LA06_n	Not Used	Not Used
p_FMC_LA07_p	Not Used	Not Used
p_FMC_LA07_n	Not Used	Not Used
p_FMC_LA08_p	ADC_SPI_CLK	ADC SPI Clock
p_FMC_LA08_n	Not Used	Not Used
p_FMC_LA09_p	Not Used	Not Used
p_FMC_LA09_n	Not Used	Not Used
p_FMC_LA10_p	CLOCK_DIR	Set the Direction of the Clock Pin
p_FMC_LA10_n	Not Used	Not Used
p_FMC_LA11_p	Not Used	Not Used
p_FMC_LA11_n	Not Used	Not Used
p_FMC_LA12_p	ADC_SDO	ADC SDO Data Output
p_FMC_LA13_p	EXT_TRIG	External Trigger
p_FMC_LA14_p	TRIGGER_DIR	Set Trigger In or Out (MDR 36 Only)
p_FMC_LA15_p	Not Used	Not Used
p_FMC_LA16_p	ADC_SYNC_n	ADC SYNC Pin
p_FMC_LA17_CC_p	Not Used	Not Used
p_FMC_LA18_CC_p	Not Used	Not Used
p_FMC_LA19_p	Not Used	Not Used
p_FMC_LA20_p	Not Used	Not Used
p_FMC_LA21_p	Not Used	Not Used
p_FMC_LA22_p	Not Used	Not Used
p_FMC_LA23_p	Not Used	Not Used

Table 6: Mezzanine Connector Pinout

A.3 VHDL Top Level Template

The sample code below gives a prototype VHDL entity declaration for the FMC I/O pins of the mezzanine. The pin naming convention on the module is as per the FMC specification.

```
--------------------------------------------------------------------------------
--        ACQ430FMC Zynq Project Top Level of Module Connection
--------------------------------------------------------------------------------
--! Standard Libraries - numeric.std for all designs
library ieee;
use ieee.std_logic_1164.all;    -- Standard Logic Functions
use ieee.numeric_std.all;   -- Numeric Functions for Signed / Unsigned Arithmetic

--! Xilinx Primitive Library
library UNISIM;
use UNISIM.VComponents.all;   -- Xilinx Primitives

--! Top Level of the ACQ430FMC Module
entity ACQ430FMC_TOP is
port(
-----------------------
--   External I/O hooks   --
-----------------------
p_FMC_CLK0_M2C_p      : inout std_logic;          --! EXT_CLK
p_FMC_CLK0_M2C_n      : inout std_logic;          --! Not Used
p_FMC_LA00_CC_p     : inout std_logic;          --! ADC_MODE_0
p_FMC_LA00_CC_n     : inout std_logic;          --! Not Used
p_FMC_LA01_CC_p     : inout std_logic;          --! Not Used
p_FMC_LA01_CC_n     : inout std_logic;          --! Not Used
p_FMC_LA02_p        : inout std_logic;          --! FP_SCL
p_FMC_LA02_n        : inout std_logic;          --! Not Used
p_FMC_LA03_p        : inout std_logic;          --! FP_SDA
p_FMC_LA03_n        : inout std_logic;          --! Not Used
p_FMC_LA04_p        : inout std_logic;          --! ADC_FSYNC
p_FMC_LA05_p        : inout std_logic;          --! TOP Deck Present - JWM to be added
p_FMC_LA06_p        : inout std_logic;          --! Not Used
p_FMC_LA07_p        : inout std_logic;          --! Not Used
p_FMC_LA08_p        : inout std_logic;          --! ADC_SPI_CLK
p_FMC_LA09_p        : inout std_logic;          --! Not Used
p_FMC_LA10_p        : inout std_logic;          --! CLOCK_DIR
p_FMC_LA11_p        : inout std_logic;          --! Not Used
p_FMC_LA12_p        : inout std_logic;          --! ADC_SDO
p_FMC_LA13_p        : inout std_logic;          --! EXT_TRIG
p_FMC_LA14_p        : inout std_logic;          --! TRIGGER_DIR
p_FMC_LA15_p        : inout std_logic;          --! Not Used
p_FMC_LA16_p        : inout std_logic;          --! ADC_SYNC_n
p_FMC_LA17_CC_p     : inout std_logic;          --! Not Used
p_FMC_LA18_CC_p     : inout std_logic;          --! Not Used
p_FMC_LA19_p        : inout std_logic;          --! Not Used
p_FMC_LA20_p        : inout std_logic;          --! Not Used
p_FMC_LA21_p        : inout std_logic;          --! Not Used
p_FMC_LA22_p        : inout std_logic;          --! Not Used
p_FMC_LA23_p        : inout std_logic           --! Not Used
);
end ACQ430FMC_TOP;
```

The ACQ430FMC board connects ADC_MODE_0 for mode control on the ADC supporting the following modes

- ADC_MODE_0 = 0, High Speed
- ADC_MODE_0 = 1, High Resolution