AO422FMC/AO422ELF Product Specification

High Performance Simultaneous Data Acquisition

 Preliminary Product Document
Subject to change

Contents

Revision History

Revision	Date	Author(s)	Description
1	06-06-2023	JMcL	Initial Version For Review
2.0	15-09-2023	JMcL	Updated with configuration options,additional performance details, and connector pin out

Glossary

- FMC : VITA57.1 FPGA Mezzanine Card
- ELF : Electrically Extended FMC, implies ULPC or DULPC (only compatible with D-TACQ carriers)
- LPC : FMC Low Pin Count standard as per VITA57.1
- ULPC : Subset by D-TACQ, Ultra Low Pin Count
- DULPC : Subset by D-TACQ, Differential Ultra Low Pin Count (ULPC with extra differential signalling)
- Xilinx ZYNQ System on Chip (SoC)
- FPGA : Field Programmable Gate Array

1 Product Description

1. AO422FMC/AO422ELF is a standard D-TACQ product, 4 channels simultaneous AO with regular buffered output on Single pin LEMO connector.
2. Standard configuration: 4 channels, 18 bit resolution, 1MSPS/channel
3. Available both as standard FMC and D-TACQ ELF standard for use with D-TACQ Carriers
4. Complies with VITA57 FMC standard, LPC version, Standard Height
5. ±10V per channel 20mA drive; ±5V soft-selectable. ±2.5V is available on the AO422ELF version used with D-TACQ Carriers.
6. Standard reconstruction filter at 50kHz. Also available in a Low-Latency Control configuration at 250kHz. Please contact info@d-tacq.com for custom options.
7. DC and AWG modes.
8. 20 bit variant available as special build.
9. TTL Sample Clock Input or Misc D/IO (FPGA programmable).
10. 5 Output version available as special build.
11. Compliant with D-TACQ ELF sites.

1.1 Product Variants

- AO422FMC-4-18 : 4 channels, 18 bit resolution
- AO422ELF-4-18 : 4 channels, 18 bit resolution
- AO422FMC-4-20 § : 4 channels, 20 bit resolution
- AO422ELF-4-20 § : 4 channels, 20 bit resolution
- AO422FMC-5-18 § : 5 channels, 18 bit resolution
- AO422ELF-5-18 § : 5 channels, 18 bit resolution
- AO422FMC-5-20 § : 5 channels, 20 bit resolution
- AO422ELF-5-20 § : 5 channels, 20 bit resolution
- § Special Build : MOQ and/or longer lead time may apply

Contact info@d-tacq.com for custom configurations. For example, the AO422FMC/AO422ELF when configured with the higher frequency reconstruction filter is has the suffix -LLC (Low Latency Control) in the product name. This is due to the typical use case, which is a control application where the best step response is required to minimise the latency.

1.2 Carrier Compatibility

The FMC module standard adds user IO to carrier modules fitted with FPGA resource. D-TACQ recommends modules based on the Xilinx ZYNQ system on chip, combining FPGA resource with a dual-core ARM Cortex A9 and gigabit Ethernet.

Compatible carriers include:

- D-TACQ ACQ1001 : D-TACQ single slot FMC carrier, Z7020
- D-TACQ ACQ1002 : D-TACQ dual slot FMC carrier, Z7020
- D-TACQ ACQ2106 : D-TACQ 6 slot FMC carrier, Z7030
- D-TACQ ACQ2206 : D-TACQ 6 slot FMC carrier, Z7030
- D-TACQ ACQ1102 : D-TACQ 2 slot FMC carrier, Z7030

- DAMC-FMC1Z7IO + D-TACQ ACQ400-MTCA-RTM-2

D-TACQ supplies a complete working Intelligent Digitizer appliance including programmable logic and microprocessor system running Linux.

2 Physical

2.1 Board Outline

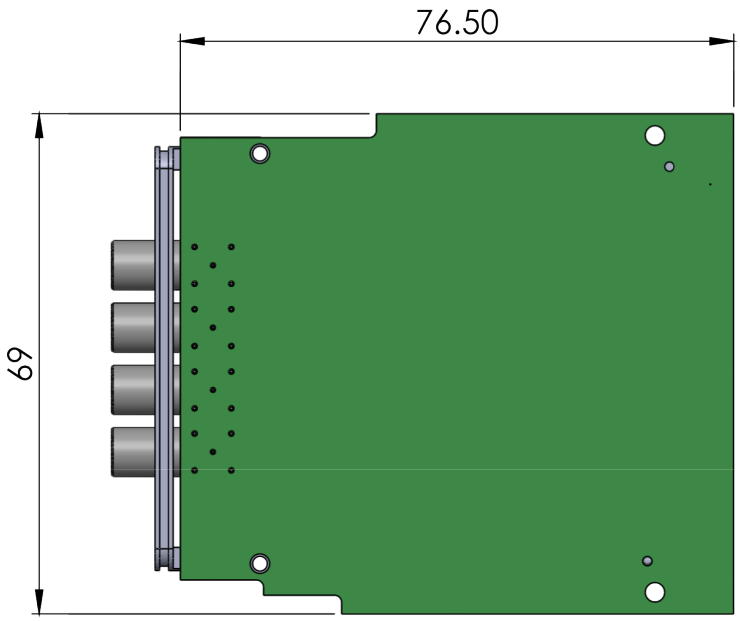

Figure 1: Board Outline

2.2 Appearance

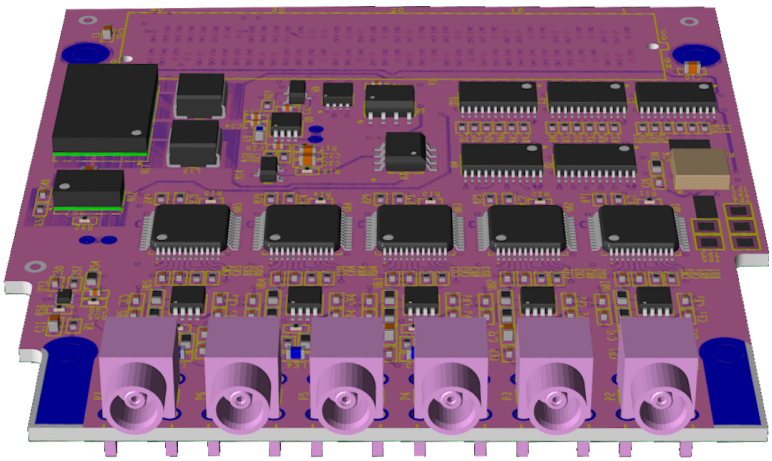

Figure 2: AO422FMC Board Outline

Note: FMC Connector omitted from the above diagram

2.3 Front Panel Connectors

- Single Pin LEMO per channel output, 4 or 5 connectors fitted
- Single Pin LEMO Front panel CLK input or Misc I/O, or use internal clock on D-TACQ Carriers.

The LEMO connectors are centre-input/shield 0V single-pin LEMO 00 Series Mini Coax connector part EPL.00.250.NTN. Mating plugs should be compatible with this part.

3 Electrical Specification

3.1 Gain Ranges

3.1.1 AO422FMC

The FMC variant has an onboard 5V master reference voltage.

Each channel has soft-selectable x1 or x2 multipliers, therefore each channel may be either:

- ±5V range
- ±10V range

3.1.2 AO420ELF

The D-TACQ ELF variant takes its master references from the carrier and is able to switch between 2.5V or 5V providing an additional output range

Each channel has soft-selectable x1 or x2 multipliers, therefore each channel may be either:

- Master reference 2.5V:
  - ±2.5V range
  - ±5V range
- Master reference 5V:
  - ±5V range
  - ±10V range

3.2 AO422FMC/ELF Analog Output Specification

#	Parameter	Value
1	Number of Channels	4 [1]
2	Sample Rate	Up to 1000 kHz, per channel simultaneous
3	Resolution	18 bits [2]
4	Coupling	DC, Single-ended Output
5	Per-Channel Maximum output current	20 mA
5	Total Maximum output current	100 mA
6	Output Voltage Range	±10V ±5V ±2.5V [3]
7	Output Impedance	33Ω
8	Offset Error	0.01% FS with numerical calibration
9	Gain Error	0.01% FS with numerical calibration
10	INL	±2 LSB
11	DNL	±1 LSB
12	THD	92 dB
13	SINAD	89 dBc
14	SFDR	95 dBc
15	SNR	90 dB
16	Full Power BW	50kHz Standard [4]
	Crosstalk	<95 dB @ 1 kHz FS
	Temperature Stability	<25 ppm/°C

[1] 5 channel version available
[2] 20 bit build option available
[3] Special build option. Please contact info@d-tacq.com for details
[4] 250kHz and 5kHz build options

Table 1: AO422FMC Output Performance

3.3 AO422FMC/ELF LEMO Clock Input, Misc I/O Specification

The Clock Input / Miscellaneous I/O has the following properties

Parameter	Value
TTL Input Low Voltage	< 1.5V [1]
TTL Input High Voltage	> 3.5V [1]
Minimum Input Voltage	> -0.5V [2]
Maximum Input Voltage	< 5.5V [2]
TTL Output Low Voltage	< 0.55V [3]
TTL Output High Voltage	> 3.8V [3]
TTL Max Output Current	24 mA

[1] Input hysteresis at least 700mV
[2] Inputs have under/over voltage protection up to 100mA
[3] Output Voltages at specified Max Current

Table 2: LEMO TTL Input/Output Characteristics

4 Mechanical & Environmental Specification

4.1 AO422FMC Mechanical & Environmental Specification

#	**Parameter**	**Value**
1	Form Factor	Standard FMC
2	Power source	External DC 12V, 300mA External DC 3.3V, 100 mA
3	Environmental	0°C - 50°C Operational -10°C - 85°C Non-Operational
4	Mezzanine Socket	Standard FMC, Low Pin Count LPC

Table 3: AO422FMC Mechanical & Environmental Specification

4.2 AO422ELF Mechanical & Environmental Specification

#	**Parameter**	**Value**
1	Form Factor	Standard FMC with ELF Pin Out
2	Power Consumption	3W Typical
3	Environmental	0°C - 50°C Operational -10°C - 85°C Non-Operational
4	Mezzanine Socket	D-TACQ ELF Pinout

Table 4: AO422ELF Mechanical & Environmental Specification

A FMC Information

A.1 I²C Devices

The board is fitted with 2 I²C devices as follows

Address	Device	Description
0x28	AD7417	Temperature Sensor and Analog Input
0x50	M24C64	Serial IPMI FRU PROM

Table 5: I²C devices

A.1.1 AD7417 Temperature Sensor

See the data sheet at AD7417

A.1.2 Serial IPMI FRU PROM

This is a standard FMC FRU devices the contents of the PROM are as per the FMC standard and the *IPMI Platform Management FRU Information Storage Definition v1.0*

Below is an example of a AO422FMC module with the serial number 10.

```
./fru-dump fru/E42200010.fru
header 0x18f0010 bia 0x18f0018
fru/E42200010.fru: manufacturer: D-TACQ Solutions
header 0x18f0010 bia 0x18f0018
fru/E46020010.fru: product-name: AO422FMC
header 0x18f0010 bia 0x18f0018
fru/E46020010.fru: serial-number: E42200010
header 0x18f0010 bia 0x18f0018
fru/E42200010.fru: part-number: AO422FMC N=4 M=44
```

A.2 FMC Connector Pin Out

FMC Pin	Signal Name	Description
p_FMC_CLK0_M2C_p	Not Used	Not Used, Dedicated Clock to Carrier FPGA
p_FMC_CLK0_M2C_n	Not Used	Not Used, Dedicated Clock to Carrier FPGA
p_FMC_CLK1_C2M_p	Not Used	Not Used, Dedicated Clock from Carrier FPGA
p_FMC_CLK1_C2M_n	Not Used	Not Used, Dedicated Clock from Carrier FPGA
p_FMC_LA00_CC_p	FMC_DAC_CLK	DAC Clock Input / Misc I/O
p_FMC_LA00_CC_n	FMC_DAC_CLK_DIR	Sample Clock / Misc I/O Direction 0 = Input 1= Output
p_FMC_LA01_CC_p	Not Used	Not Used
p_FMC_LA01_CC_n	Not Used	Not Used
p_FMC_LA02_p	DAC_RANGE(1)	DAC 1 Range Select
p_FMC_LA02_n	DAC_RANGE(2)	DAC 2 Range Select
p_FMC_LA03_p	DAC_RANGE(3)	DAC 3 Range Select
p_FMC_LA03_n	DAC_RANGE(4)	DAC 4 Range Select
p_FMC_LA04_p	DAC_RANGE(5)	DAC 5 Range Select
p_FMC_LA04_n	DAC_REF_RANGE	Switch Reference Voltage (ELF Version only
p_FMC_LA05_p	DAC_RST_n	DAC Reset to all DACs
p_FMC_LA05_n	Not Used	Not Used
p_FMC_LA06_p	Not Used	Not Used
p_FMC_LA06_n	Not Used	Not Used
p_FMC_LA07_p	DAC_LD_n	DAC Load Strobe
p_FMC_LA07_n	Not Used	Not Used
p_FMC_LA08_p	DAC_SDO(1)	SPI Data out from DAC 1
p_FMC_LA08_n	Not Used	Not Used
p_FMC_LA09_p	DAC_SDO(2)	SPI Data out from DAC 2
p_FMC_LA09_n	Not Used	Not Used
p_FMC_LA10_p	DAC_SDO(3)	SPI Data out from DAC 3
p_FMC_LA10_n	Not Used	Not Used
p_FMC_LA11_p	DAC_SDO(4)	SPI Data out from DAC 4
p_FMC_LA11_n	Not Used	Not Used
p_FMC_LA12_p	DAC_SDO(5)	SPI Data out from DAC 5
p_FMC_LA13_p	DAC_SDI(1)	SPI Data in to DAC 1
p_FMC_LA14_p	DAC_SDI(2)	SPI Data in to DAC 2
p_FMC_LA15_p	DAC_SDI(3)	SPI Data in to DAC 3
p_FMC_LA16_p	DAC_SDI(4)	SPI Data in to DAC 4
p_FMC_LA17_CC_p	DAC_SDI(5)	SPI Data in to DAC 4
p_FMC_LA18_CC_p	DAC_SYNC_n(1)	SYNC signal to DAC 1
p_FMC_LA19_p	DAC_SYNC_n(2)	SYNC signal to DAC 2
p_FMC_LA20_p	DAC_SYNC_n(3)	SYNC signal to DAC 3
p_FMC_LA21_p	DAC_SYNC_n(4)	SYNC signal to DAC 4
p_FMC_LA22_p	DAC_SYNC_n(5)	SYNC signal to DAC 5
p_FMC_LA23_p	DAC_SPI_CLK	SPI Clock to All DACs

Table 6: FMC Connector Pin Out